

1200 Baud Modem

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Description

The modem on the reverse side is a 1200 baud frequency-shift-keyed (FSK) modem utilizing 2200 Hz for the *mark* tone and 1200 Hz for the *space* tone. (Note that the non-return-to-zero-incremental (NRZI) modulation format used by the Vancouver board is insensitive to the polarity of the signal; it is only the *transitions* which are important.) The receive section of the modem consists primarily of a four-pole bandpass filter, a diode limiter, a 565 phase-locked loop, a six-pole lowpass filter, and a slicer. In addition, a threshold detector clamps the output level to a mark in the absence of any input signal. The bandpass filter rejects noise outside of the 1200-2200 Hz passband, and the 600 Hz lowpass filter rejects the VCO signal and its harmonics from the demodulated signal.

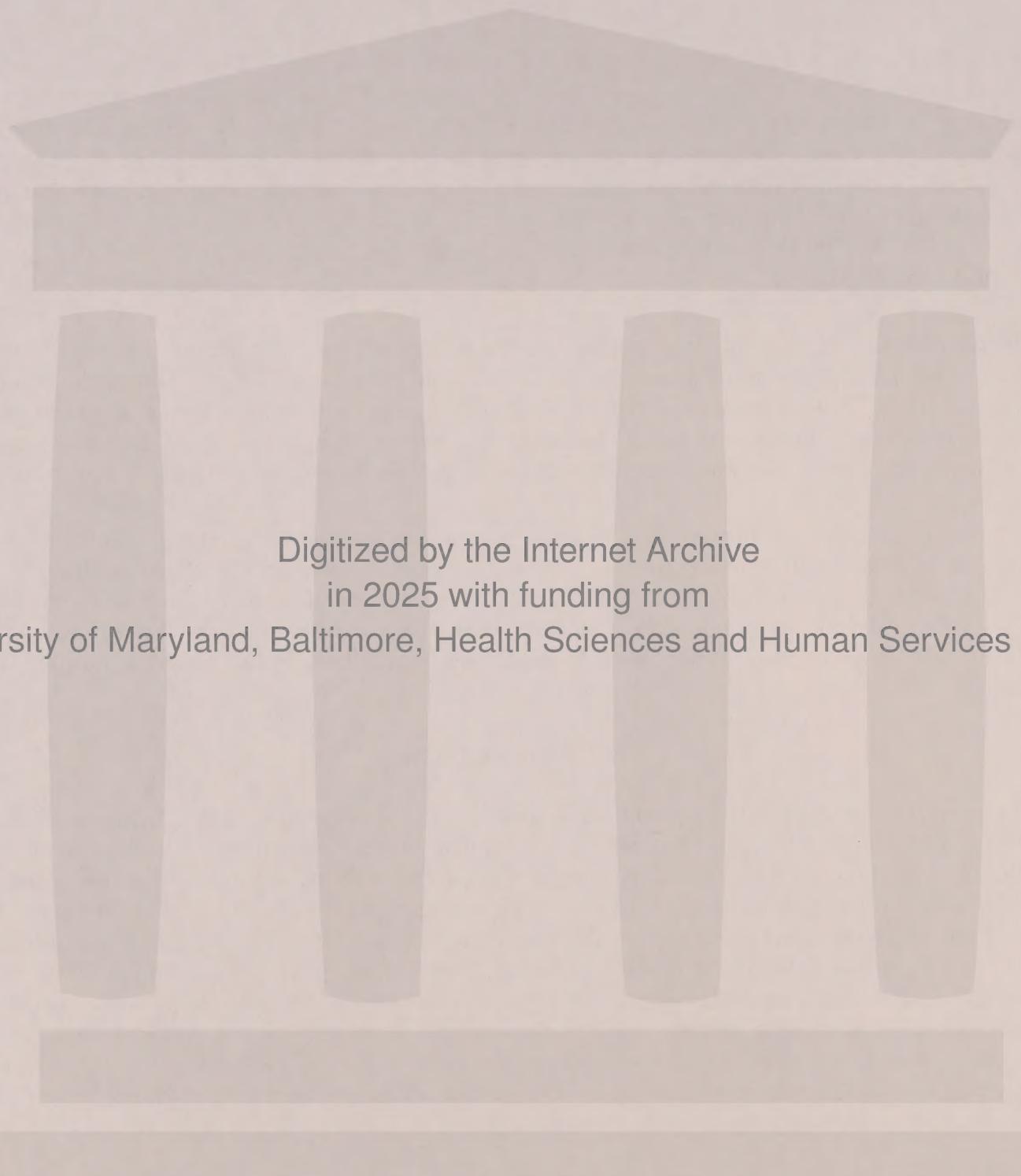
The transmit section of the modem consists of a fixed-frequency oscillator operating at approximately 109 kHz, a divide-by 5 or 9 counter, a decade divider, a D/A converter, and a two-pole lowpass filter. (The ratio between 1200 and 2200 Hz is within about 2% of 5/9.) The D/A converter, consisting of 4 resistors and the divide-by-10 Johnson counter, provides a 10-point, 5-level approximation to a sine wave whose harmonics are easily filtered out. The output waveform is phase-continuous at the frequency transitions.

The op-amps can be inexpensive 1458's; these provide two independent sections requiring no external compensation in an 8-pin mini-dip package. All 4000-series numbers are CMOS logic chips. All active devices -- the op-amps, the 565, and the CMOS chips -- are connected between +5 V and -5 V for power. The frequency-determining components should be as accurate as possible. One percent resistors and 5% capacitors are recommended, although units have been successfully built using 1% resistors and 10% capacitors.

Adjustment

The receiver input level should be adjusted so that the level of the signal at point A (just before the diode limiter) is a couple of volts RMS, but not high enough so that the op-amp starts to clip. With the input frequency set to about 1700 Hz, adjust the *Receive Frequency* pot for balanced output at pins 6 and 7 of the 565. Then tentatively adjust the *Decision Level* pot for zero output from the EIA OUT pin (this will be noisy with a fixed-frequency input signal right at the decision threshold). Next, connect a FSK signal to the input (the beacon signal from the packet repeater is a good source, if you work fast on the next step). Using an oscilloscope, adjust the *Decision Level* pot for equal-width *mark* and *space* levels for those portions of the input waveform having only one bit-cell at each frequency. (It may take a couple of tries to get this adjustment correct, and there is some interaction between the *Receive Frequency* and the *Decision Level* controls.) The *Threshold* pot should be adjusted so that the decision point corresponds roughly to the level at which the diodes start to clip the signal going to the 565.

The only adjustment to the transmitter section is the *Transmit Frequency*. Adjust this pot so that the oscillator frequency is approximately 109 kHz, or adjust the frequency so that the CARRIER OUT signal is as close to 1200 Hz and 2200 Hz as possible. Alternatively, assuming that the receiver has been properly adjusted, it is possible to use the receiver section to adjust the transmitter frequency. Feed the transmitter output to the receiver input, connect a data source or a 1200 Hz square wave to the EIA IN pin, and adjust the *Transmit Frequency* pot for equal-width *mark* and *space* levels at the EIA OUT pin of the receiver.



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